Main Directions of Riga Event Timer Development and Current Results

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The main directions of Riga Event Timer (ET) development include:

1. Supporting of stable precision at the level 3 ps RMS in a wide temperature range by means of:
    - temperature compensation,
    - fast and robust calibration.

2. More compact design, more fast operating by means of:
    - integration of all digital functions in one FPGA,
    - higher clock frequency,
    - high-speed PC interfaces: USB3, PCIe, Ethernet 1G, etc;

3. User interface friendliness:
    - user get the time-stamps directly from hardware, without any additional data processing by PC

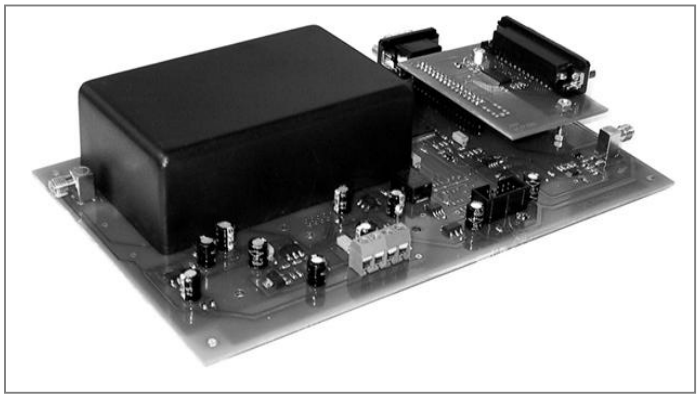
Up to now the first direction is considerably advanced, while other directions are at the beginning stage of development

1. The best and stable precision – temperature stabilization

The Riga ETs offer the best precision directly after calibration in steady-state operating conditions. Thereafter an ambient temperature variation can impair the best precision.

The problem is to provide nearly-best precision without re-calibration in a wide range of ambient temperature changing.

Our first experiments showed that traditional thermostating is not the best solution in terms of the ET hardware simplicity, compactness and power consuming.

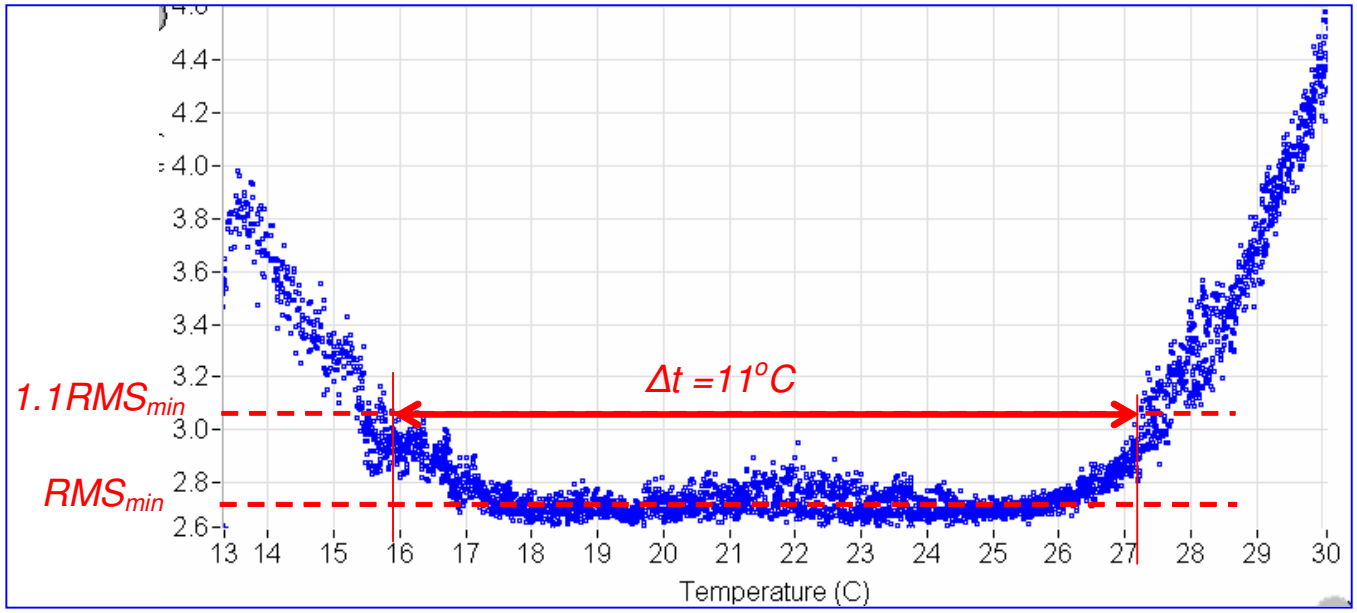


Thermostat with heating

Thermostat with cooling

Therefore other solutions of the problem were investigated

Unlike the temperature stabilization, right temperature compensation leads to sufficiently effective solution



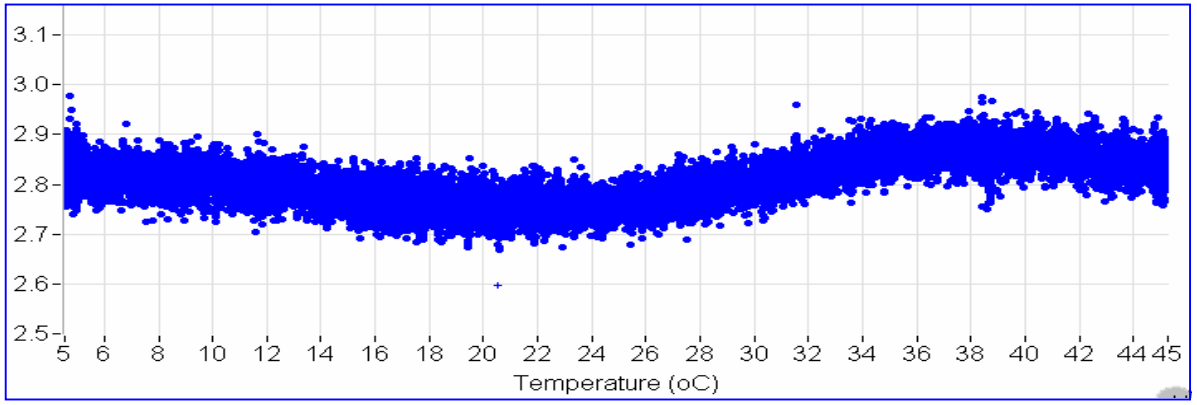
RMS error vs ambient temperature [°C]

As compared with the A032-ET and early A033-ET realizations, temperature range Δt now is essentially wider.

1. The best and stable precision – robust calibration

When ambient temperature is considerable changed, the Riga ET should be re-calibrated. Conventionally we use for calibration a stand-alone crystal clock oscillator with “right” calibration frequency that provides the best ET precision. In this case the temperature drift of the “right” frequency causes sometimes improper quality of calibration and may require a repeating calibration.

Unlike the earlier used solution, FLL- and PLL-based synthesis of the “right” frequency always provides the best quality of calibration in a wide temperature range



RMS error after re-calibrations with use of PLL synthesizer

1. The best and stable precision – calibration tables swapping

It is possible to create preliminary the calibration tables for different temperature ranges of the ET operation, and automatically select one of the tables, taking into account the current temperature. Evident advantage of this approach is actual exclusion of the ET calibration as a complicated online operation.

Practicability of this approach has been experimentally confirmed. It seems that, in combination with the right temperature compensation, this approach will allow to considerably improve precision characteristics of the Riga ETs

Development areas:

All digital functions into one FPGA:
- large buffer memory;
- calibration functions and tables;
- interface function with PC;
- gate prediction and arming;
- conditioning control and adaptation;
- ADC samples conversion to time;
- time scale support and substitution.

Higher clock frequency has restrictions:
ADC quality versus speed,
FPGA safety versus speed

High-speed PC interfaces:
USB3 – 400 Mbyte/s
PCIe – from 250 Mbyte/s up to 1Gbyte/s
Ethernet – from 12 Mbyte/s up to 3Gbyte/s
etc;

Objectives:

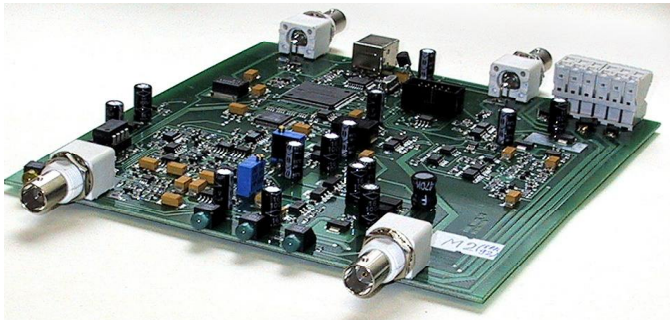
Integration of timing related digital functions into a single FPGA will allow to make the timer hardware more reliable and compact, with lower power consumption

Higher clock will allow to increase the performance: better RMS, shorter “dead time”

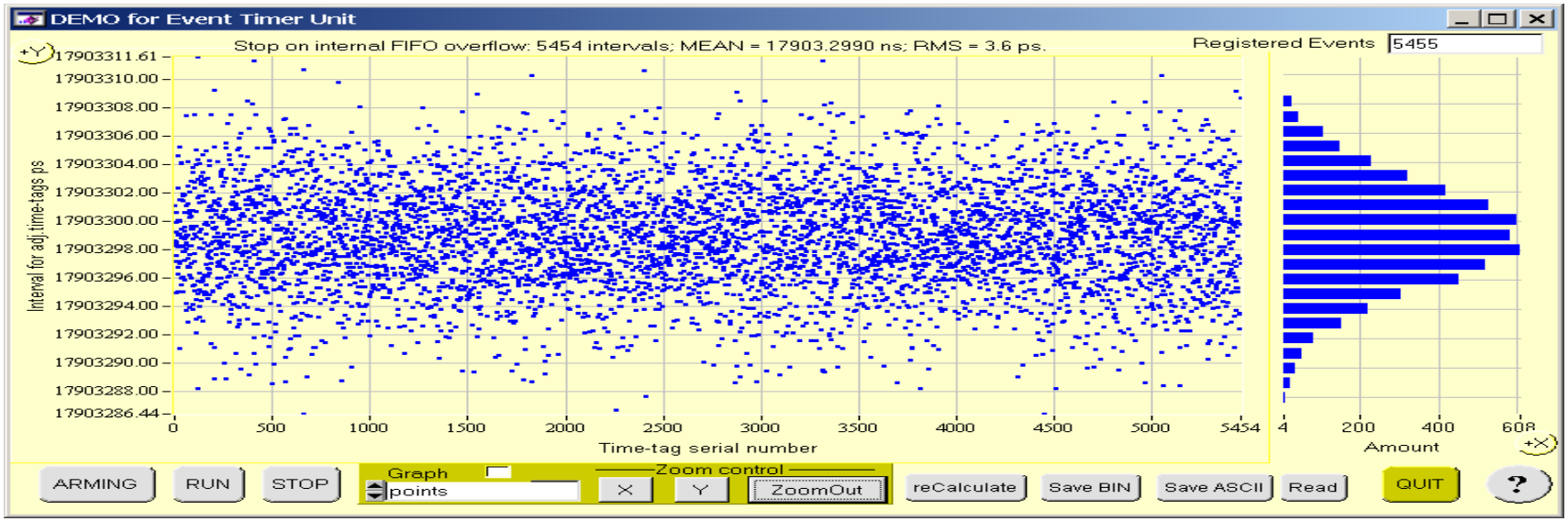
High-speed interface will allow to increase the average event frequency and extend gate control functionality

2. More compact, more fast realization – first results

Compact Timer

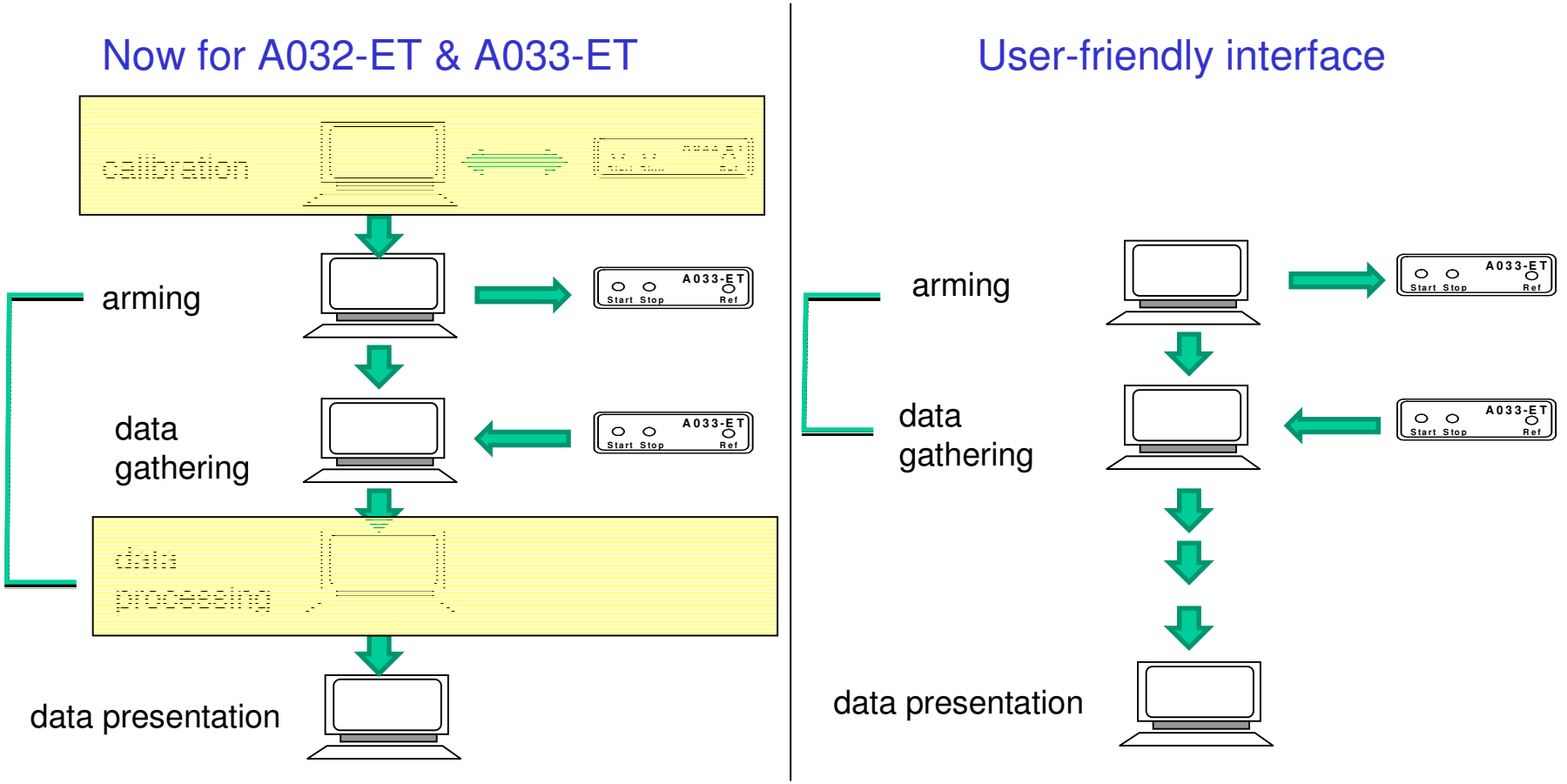


Event freq.avr	**up to 1 MHz**
Event freq.burst	**up to 20 MHz**
RMS	**3-5 ps**
PC Interface	**USB2**
Size (mm)	**130x110x20**
Power	**6 W**



Measured intervals and deviation histogram

3. User interface friendliness



Conclusions

We have defined three main directions of further Riga Event Timer development, based on our view of SLR problems:

- the best and stable precision
- more compact, more fast realization
- user interface friendliness

Some results are already achieved such as single-shot RMS resolution less than 3 ps, weakened dependence on temperature, robust calibration independents on temperature variation, modular design with USB2 interface.

Thank you!